Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of claims:

1. (Original) An integrated circuit comprising:

a substrate;

a top conductive layer, the top conductive layer having at least one bonding pad and a sub-layer of relatively stiff material;

one or more intermediate conductive layers formed between the top conductive layer and the substrate;

layers of insulating material separating the conductive layers from each other, one layer of the layers of insulating material is relatively hard and is located between the top conductive layer and an intermediate conductive layer closest to the top conductive layer; and

devices formed in the integrated circuit, wherein at least the intermediate conductive layer closest to the top conductive layer is adapted for functional interconnections of select devices under the bond pad.

2. (Original) The integrated circuit of claim 1, wherein the sub-layer is made of TiN.

3 (Original) The integrated circuit of claim 1, wherein the sub-layer is made of TiW.

4. (Original) The integrated circuit of claim 1, where the sub-layer is a layer of nitride.

5. (Original) The integrated circuit of claim 1, wherein the devices are relatively high current devices and the one or more intermediate conductive layers are formed into relatively wide interconnect lines to accommodate relatively high currents.

6. (Original) The integrated circuit of claim 1, wherein at least one of the conductive layers further comprises:

conductive sub-layers formed by a sub-micron process.

7. (Original) The integrated circuit of claim 1, wherein the conductive layers are metal layers.

8. (Original) The integrated circuit of claim 7, wherein at least one of the metal layers are formed from a metal layer from a group of metal layers comprising aluminum and copper.

9. (Original) The integrated circuit of claim 1, wherein the one or more intermediate conductive layers further comprises:

a second conductive layer, the second conductive layer separated from the top conductive layer by a relatively thick insulating layer.

10. (Currently amended) The integrated circuit of claim 9, wherein the relatively thick insulating layer is an oxide layer that is at least 1.5 ~~u~~μm thick.

11. (Original) The integrated circuit of claim 9, wherein the second conductive layer further comprises:

a layer of TiN positioned adjacent the relatively thick insulation layer.

12. (Original) The integrated circuit of claim 9, wherein the second conductive layer has gaps.

13. (Original) The integrated circuit of claim 12 wherein the gaps take up no more than 10% of the total area of the second metal layer under the at least one bond pad.

14. (Original) The integrated circuit of claim 12, wherein the gaps are orientated to minimize the impact on current flow through the second metal layer.

15. (Original) An integrated circuit comprising:

a substrate;

device regions formed on and in the substrate;

a top metal layer, the top metal layer having one or more bonding pads formed thereon, the device regions located between the substrate and the top metal layer;

a second metal layer located between the top metal layer and the device regions; and

a layer of relatively thick insulating material separating the top metal layer from the second metal layer, wherein the relatively thick insulating layer is adapted to resist cracking.

16. (Currently amended) The integrated circuit of claim 15, wherein the relatively thick insulating layer is a layer of oxide having a thickness of at least 1.5 ~~u~~μm.

17. (Original) The integrated circuit of claim 15, further including:

one or more intermediate metal layers located between the device regions and the second metal layer.

18. (Original) The integrated circuit of claim 15, wherein the second metal layer includes a sub-layer of TiN located adjacent the layer of relatively thick insulating material.

19. (Original) The integrated circuit of claim 15, wherein the second metal layer has gaps adapted to strengthen the integrated circuit.

20. (Original) The integrated circuit of claim 19, wherein the gaps take up no more than 10% of the total area of the second metal layer under the one or more bonding pads.

21. (Currently amended) The integrated circuit of claim 19, wherein the gaps are orientated to ~~minimizes~~ minimize the impact on current flow through the second metal line.

22. (Original) The integrated circuit of Claim 15, further comprising:

a layer of relatively stiff material adapted to distribute both lateral and vertical stresses over a larger area of the relatively thick insulating layer.

23. (Currently amended) The integrated circuit of Claim 22, wherein the layer of relatively stiff material is formed adjacent the top metal layer and the relatively thick insulating layer.

24. (Original) The integrated circuit of claim 22, wherein the layer of relatively stiff material is made of TiN.

25. (Original) The integrated circuit of claim 22, wherein the layer of relatively stiff material is made of TiW.

26. (Original) The integrated circuit of claim 22, wherein the thickness of the relatively stiff material is approximately 80nm.

27. (Currently amended) The integrated circuit of claim 22, wherein the layer of relatively stiff material ~~if~~ is a layer of nitride.

28. (Original) The integrated circuit of claim 22, wherein the layer of relatively stiff material is a sub-layer of the top metal layer formed by a sub-micron process.

29. (Original) The integrated circuit of claim 28, wherein the sub-layer of relatively stiff material is formed near the relatively thick insulating layer.

30. (Original) An integrated circuit comprising:

a substrate;

a plurality of devices formed on and in the substrate;

a top metal layer having at least one bond pad formed on a surface of the top metal layer;

a second metal layer located between the top metal layer and the substrate, the second metal layer having gaps adapted to strengthen the integrated circuit; and

a first layer of insulating material formed between the top metal layer and the second metal layer.

31. (Original) The integrated circuit of claim 30, wherein the density of the gaps in the second metal layer is minimized to minimize the impact on the function of the integrated circuit.

32. (Original) The integrated circuit of claim 30, wherein the gaps take up no more than 10% of the total area of the second metal line under an associated bond pad.

33. (Original) The integrated circuit of claim 30, wherein the gaps extend in a direction of a current flow.

34. (Original) The integrated circuit of claim 30, wherein the top metal layer includes a relatively stiff sub-layer located adjacent the first insulating layer.

35. (Original) The integrated circuit of claim 30, wherein the second metal layer includes a TiN sub-layer located adjacent the first insulating layer.

36. (Original) The integrated circuit of claim 30, wherein the second metal layer includes a TiW sub-layer located adjacent the first insulating layer.

37. (Original) The integrated circuit of claim 30, wherein the first insulating layer is relatively thick.

38. (Currently amended) The integrated circuit of claim 37, wherein the first insulating layer is a first oxide layer having a thickness of at least 1.5 ~~u~~μm.

39. (Currently amended) A method of forming an integrated circuit with ~~active~~ circuitry under a bond pad, the method comprising:

forming devices in and on a substrate;

forming a first metal layer;

forming a first layer of relatively thick insulating material overlaying the first metal layer, wherein the thickness of the first insulating layer strengthens the integrated circuit;

forming a top metal layer overlaying the relatively thick insulating layer; and

forming a bond pad on a surface of the top layer.

40. (Currently amended) The method of claim 39, wherein the first layer of relatively thick insulating material is a layer of oxide having a thickness of at least 1.5 ~~u~~μm thick.

41. (Original) The method of claim 39, further comprising;

forming one or more intermediate metal layers between the devices and the first metal layer.

42. (Original) The method of claim 39, wherein forming the first metal layer further comprises:

patterning the first metal layer to form gaps.

43. (Original) The method of claim 42, wherein the gaps take up no more than 10% of the total area of the first metal layer under the bond pad.

44. (Original) The method of claim 42, wherein the gaps are formed to be oriented such that the impact on the current flow through the first metal layer is minimized.

45. (Original) The method of claim 42, wherein the gaps are formed to extend in a direction of a current flow in the first metal layer.

46. (Original) The method of claim 39, wherein forming the top metal layer, further comprises:

forming a sub-layer of relatively stiff material.

47. (Original) The method of claim 46, wherein the relatively stiff material TiN.

48. (Original) The method of claim 46, wherein the relatively stiff material is made from a layer of nitride.

49. (Original) The method of claim 46, wherein the relatively stiff material is formed near the first layer of relatively thick insulating material.

50. (Currently amended) A method of forming an integrated circuit, the method comprising;

forming device regions ~~is~~ in a substrate;

depositing a first metal layer overlaying the device regions;

pattering the first metal layer to form gaps, wherein the gaps extend in a current flow direction;

forming an insulating layer overlaying the first metal layer and filling in the gaps, wherein the gaps strengthen the integrated circuit by providing pillars of harder insulating material;

depositing a top layer of metal overlaying the insulating layer; and

forming a bond pad on a surface of the top layer of metal.

51. (Currently amended) The method of claim 50, wherein the insulating layer is a layer of oxide that is at least 1.5 ~~u~~μm thick.

52. (Original) The method of claim 50, wherein the gaps in the first metal layer take up no more than 10% of the total area of the metal line under the bond pad.

53. (Original) The method of claim 50, wherein forming the top metal layer further comprises:

forming a sub-layer of relatively stiff material adjacent the insulating layer.

54. (Original) The method of claim 53, wherein the relatively stiff material is TiN.

55. (Original) The method of claim 53, wherein the relatively stiff material is TiW.

56. (Original) The method of claim 53, wherein the relatively stiff material is made from a sub-layer of nitride.

57. (Original) A method of forming an integrated circuit, the method comprising:

forming device regions in and on a substrate;

forming a first metal layer overlaying the device regions;

forming an insulating layer overlaying the first metal region;

forming a top metal layer overlaying the insulating layer including a sub-layer of relatively stiff material near the insulating layer; and

forming a bonding pad on a surface of the top metal layer.

58. (Original) The method of claim 57, wherein the sub-layer of relatively thick material is TiN.

59. (Original) The method of claim 57, wherein the relatively stiff material is TiW.

60. (Currently amended) The method of claim 57, wherein the sub-layer of the relatively thick material is ~~s~~ formed ~~form~~ from a layer of nitride.

61. (Currently amended) The method of claim 57, wherein the insulating layer is an oxide layer having thickness of not less than 1.5 ~~u~~μm.

62. (Original) The method of claim 57, wherein forming the first metal layer further comprises:

patterning the first metal layer to form gaps, wherein the gaps take up no more than 10% of a total layer area of the first metal layer under the bond pads.

63. (Original) The method of claim 57, further comprising:

forming one or more intermediate metal layers between the first metal layer and the device regions; and

patterning the one or more intermediate metal layers to form interconnects between the devices.

64. (New) The integrated circuit of claim 14, wherein the gaps being orientated to minimize the impact on the current flow through the second metal layer, further comprises:

extending the gaps in the direction of the current flow.

65. (New) The integrated circuit of claim 21, wherein the gaps being orientated to minimize the impact on the current flow through the second metal layer, further comprises:

extending the gaps in the direction of the current flow.

66. (New) The method of claim 39, wherein forming devices in and on a substrate includes forming at least one of the devices under the bond pad.

67. (New) The method of claim 50, wherein the bond pad is formed directly over at least one of the device regions.

68. (New) An integrated circuit comprising:

a substrate;

a top conductive layer, the top conductive layer having at least one bonding pad and at least one sub-layer wherein the at least one sub-layer is relatively more stiff than the other sub-layers of the top conductive layer;

one or more intermediate conductive layers formed between the top conductive layer and the substrate;

one or more layers of insulating material separating the one or more conductive layers from each other; and

devices formed in the integrated circuit, wherein at least the intermediate conductive layer closest to the top conductive layer is adapted for functional interconnections of select devices under the bond pad.

69. (New) The integrated circuit of claim 68, wherein the at least one sub-layer is one from a group comprising TiN, SiN and TiW.

70. (New) The integrated circuit of claim 68, wherein at least one of the intermediate conductive layers has gaps.

71. (New) The integrated circuit of claim 70, wherein the gaps extend in a direction of current flow to minimize their impact on current flow.

72. (New) The integrated circuit of claim 68, wherein the at least one of the intermediate conductive layers is the intermediate conductive layer closest the top conductive layer.

73. (New) The integrated circuit of claim 68, wherein one layer of the layers of insulating material is thicker than the other layers of insulating material and is located between the top conductive layer and an intermediate conductive layer closest to the top conductive layer.

74. (New) An integrated circuit comprising:

a substrate;

device regions formed on and in the substrate;

a top metal layer, the top metal layer having one or more bonding pads formed thereon, the device regions located between the substrate and the top metal layer;

a second metal layer located between the top metal layer and the device regions; and

a first layer of insulating material separating the top metal layer from the second metal layer, wherein the insulating layer has a thickness selected to resist cracking.

75. (New) The integrated circuit of claim 74, wherein the layer of insulating material is at least 1.5μm thick.

76. (New) The integrated circuit of claim 74, wherein the second metal layer has one or more gaps extending in the direction of current flow.

77. (New) The integrated circuit of claim 74, further comprising:

a plurality of intermediate metal layers between the top metal layer and the substrate, the plurality of metal layers including the second metal layer; and

layers of insulating material separating the conductive layers from each other, the layers of insulating material including the first layer of insulating material.

78. (New) The integrated circuit of claim 77, wherein the plurality of intermediate conductive layers under the one or more bonding pads are adapted for active devices and functional interconnections.

79. (New) An integrate circuit comprising:

a substrate;

a top conductive layer, the top conductive layer having at least one bonding pad formed thereon;

one or more intermediate conductive layers formed between the top conductive layer and the substrate;

one or more layers of insulating material separating the one or more conductive layers from each other;

one of the one or more intermediate conductive layers closest the top conductive layer having gaps adapted to strengthen the integrated circuit; and

devices formed in the integrated circuit, wherein the one or more intermediate conductive layers are adapted for functional interconnections of select devices under the bond pad.

80. (New) The integrated circuit of claim 79, further comprising:

a sub-layer of relatively stiff material that is stiffer than the top conductive layer, the sub-layer of relatively stiff material formed between the top conductive layer and one of the one or more layers of insulation material separating the at least one intermediate conductive layer closest to the top conductive layer.

81. (New) The integrated circuit of claim 79, wherein one layer of the layers of insulating material is thicker than the other layers of insulating material and is located between the top conductive layer and an intermediate conductive layer closest to the top conductive layer.

82. (New) The integrated circuit of claim 79, wherein the gaps in the one of the one or more intermediate conductive layers closest the top conductive layer extend in a direction of current flow to minimize their impact on current flow.

83. (New) The integrated circuit of claim 79, wherein the gaps in the one of the one or more intermediate conductive layers closest the top conductive layer take up no more than 10% of the area under the at least one bonding pad.

84. (New) An integrated circuit comprising:

a substrate;

a top conductive layer, the top conductive layer having at least one bonding pad formed thereon and at least one sub-layer wherein the at least one sub-layer is relatively more stiff than the remaining top conductive layer;

one or more intermediate conductive layers formed between the top conductive layer and the substrate, one of the one or more intermediate conductive layers closest the top conductive layer having gaps adapted to strengthen the integrated circuit;

one or more layers of insulating material separating the one or more conductive layers from each other, the one or more layers of insulating material including a first layer of insulating material separating the top metal layer from the closest one of the one or more intermediate conductive layers, wherein the insulating layer has a thickness selected to resist cracking; and

devices formed in the integrated circuit, wherein the one or more intermediate conductive layers under the at least one bonding pad are adapted for active devices and functional interconnections.

85. (New) A method of forming an integrated circuit, the method comprising:

forming devices on and in a substrate;

forming one or more intermediate conductive layers overlaying the substrate;

forming one or more layers of insulating material separating the one or more conductive layers from each other;

forming a top conductive layer, the top conductive layer including at least one sub-layer of material that is relatively more stiff than the remaining top conductive layer; and

forming at least one bonding pad on the top conductive surface, wherein the at least one sub-layer of material that is relatively stiff is adapted to prevent the cracking of the one of more intermediate conductive layers under the at least one bonding pad so that one or more intermediate conductive layers under the at least one bonding pad can be used for functional interconnections of selected ones of the devices.

86. (New) The method of claim 85, wherein the sub-layer that is relatively stiff is made from one from a group of materials comprising TiN, SiN and TiW.

87. (New) The method of claim 85, further comprising:

forming one of the one or more layers of insulating material between the top conductive layer and an intermediate conductive layer closest the top conductive layer to be relatively thicker than the remaining one of more layers of insulation.

88. (New) The method of claim 85, further comprising:

forming gaps an in one of the one or more intermediate conductive layers to form pillars of relatively stiff insulating material passing through the one of the one or more intermediate conductive layers.

89. (New) The method of claim 88, wherein the one of the one or more intermediate conductive layers is the intermediate conductive layer closest the top conductive layer.

90. (New) A method of forming an integrated circuit, the method comprising:

forming device regions on and in a substrate;

forming a first metal layer overlaying the substrate;

forming a top metal layer overlaying the first metal layer;

forming at least one bonding pad on the top metal layer; and

forming a first layer of insulating material separating the top metal layer from the first metal layer, wherein the first layer of insulating material has a thickness selected to resist cracking.

91. (New) The method of claim 90, wherein the first layer of insulating material is formed to be at least 1.5μm thick.

92. (New) The method of claim 90, further comprising:

forming one or more intermediate metal layers between the first metal layer and the substrate; and

forming one or more insulation layers to separate the one or more intermediate metal layers form each other.

93. (New) The method of claim 90, further comprising;

forming a sub-layer of material between the top metal layer and the first layer of insulating material, the sub-layer of material being relatively more stiff than the remaining top metal layer such that stresses on the top metal layer that occur during the formation of the one or more bonding pads are distributed over a larger area of the first layer of insulating material to reduce the probability of cracking the first layer of insulating material.

94. (New) The method of claim 90, further comprising:

forming gaps in the first metal layer to form pillars of relatively stiff insulating material passing through the first metal layer.

95. (New) A method of forming an integrated circuit, the method comprising:

forming devices in and on a substrate;

forming a top conductive layer overlaying the substrate;

forming at least one bonding pad on the top conductive layer;

forming one or more intermediate conductive layers between the top conductive layer and the substrate;

forming one or more layers of insulating material separating the one or more conductive layers from each other; and

forming gaps in one of the one or more intermediate conductive layers closest the top conductive layer, the gaps being adapted to prevent cracking of the one or more intermediate conductive layers under the at least one bond pad by forming pillars of relatively stiff insulation material passing through the one of the one or more intermediate conductive layers closest the top conductive layer, wherein the one or more intermediate conductive layers are adapted for functional interconnections of select devices under the bond pad.

96. (New) The method of claim 95, wherein the gaps in the one of the one or more intermediate conductive layers closest the top conductive layer and formed in the direction of the current flow to reduce the effect of the gaps on the current flow.

97. (New) The method of claim 95, further comprising:

forming a sub-layer of material between the top conductive layer and one of the layers of insulating material separating the one of the one or more intermediate conductive layers closest the top conductive layer from the top conductive layer, the sub-layer of material being relatively more stiff than the remaining top conductive layer such that stresses on the top conductive layer that occur during the formation of the at least one bonding pad are distributed over a larger area of the one or more layers of insulating material to reduce the probability of cracking the one or more layers of insulating material.

98. (New) The method of claim 95, further comprising:

forming one of the one or more layers of insulating material between the top conductive layer and an intermediate conductive layer closest the top conductive layer to be relatively thicker than the remaining one of more layers of insulation.